Energy-Efficient AI Chip Designs with Digital and Analog Circuits

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Abstract: AI algorithms have been widespread across many practical applications, e.g. convolutional neural networks (CNNs) for computer vision, long short-term memory (LSTM) for speech recognition, etc., but state-of-the-art algorithms are compute-/memory-intensive, posing challenges for AI hardware to perform inference and training tasks with high throughput and low power consumption, especially on area-/energy-constrained edge devices.

In this talk, I will present our recent research of several energy-efficient AI ASIC accelerators on both all-digital chips and analog/mixed-signal circuit based chips. These include (1) a 40nm CNN inference accelerator with conditional computing and low external memory access, (2) a 28nm CNN training accelerator exploiting dynamic activation/weight sparsity, and (3) a 28nm programmable in-memory computing (IMC) inference accelerator integrating 108 capacitive-coupling-based IMC SRAM macros. We will discuss the digital/analog circuits and architecture design, as well as hardware-aware algorithms employed for the proposed energy-efficient AI accelerators. Based on the demonstrated advantages and challenges of digital and analog AI chip designs, emerging research directions for new AI hardware with new device/circuit/architecture/algorithm design considerations will be discussed.

Biography: Jae-sun Seo received the Ph.D. degree from the University of Michigan, Ann Arbor in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center, working on the DARPA SyNAPSE project and next-generation processor designs. Since 2014, he has been with Arizona State University, where he is currently an Associate Professor in the School of ECEE. He was a visiting faculty at Intel Circuits Research Lab in 2015. His research interests include efficient hardware design of machine learning algorithms and neuromorphic computing. Dr. Seo was a recipient of IBM Outstanding Technical Achievement Award (2012), NSF CAREER Award (2017), and Intel Outstanding Researcher Award (2021). He has served on the technical program committees for ISSCC, MLSys, DAC, DATE, ICCAD, etc.